IN THE CLAIMS

Please amend the claims as follows:

Claim1 (Currently Amended): A digital system that carries out digital processing in accordance with a single or a plurality of digital clock signals to perform a prescribed basic function, the digital system comprising [[,]] :

a plurality of delay elements provided therein each comprising a circuit element ~~that~~ configured to change ~~changes~~ a delay time according to a value indicated by a control signal, the circuit element ~~and is~~ inserted in each of a plurality of clock circuits that supply the clock signals, and

a plurality of holding circuits ~~that~~ configured to hold a plurality of control signals applied to the plurality of delay elements, ~~characterized in that~~ wherein, in a state in which the digital system is supplied with power from a variable output voltage power supply apparatus, values of the plurality of control signals held by the plurality of holding circuits are changed by an external apparatus in accordance with a probabilistic search technique so that a basic function of the digital system satisfies prescribed specifications.

Claim 2 (Currently Amended): The digital system described in claim 1, ~~characterized in that~~ wherein values of control signals held in the holding circuits are sequentially changed by the external apparatus in accordance with a genetic algorithm in a search for optimal values that brings the digital system into a state where its basic function satisfies prescribed specifications.

Claim 3 (Currently Amended): The digital system described in claim 1, ~~characterized~~

~~in that~~ wherein values of control signals held in the holding circuits are sequentially changed by the external apparatus in accordance with genetic programming in a search for optimal values that brings the digital system into a state where its basic function satisfies prescribed specifications.

Claim 4 (Currently Amended): The digital system ~~described in any~~ of ~~claims~~ claim 1 ~~to 3~~, ~~characterized in that~~ wherein the change to the plurality of control signals by the external apparatus is performed while changing an output voltage of the power supply apparatus in steps.

Claim 5 (Currently Amended): The digital system ~~described in any~~ of ~~claims~~ claim 1 ~~to 3~~, ~~characterized in that~~ wherein the change to the plurality of control signals by the external apparatus is performed with an output voltage of the power supply apparatus in a state of being lower than a design value of the digital system.

Claim 6 (Currently Amended): A digital system that carries out digital processing in accordance with a single or a plurality of digital clock signals to perform a prescribed basic function, characterized in that the digital system comprises[[,]] :

a plurality of delay elements provided therein, each comprising a circuit element that changes a delay time according to a value indicated by a control signal and is inserted in each of a plurality of clock circuits that supply the clock signals[[,]] ;

a plurality of holding circuits that hold a plurality of control signals applied to the plurality of delay elements[[,]] ; and

a setting means that in a state in which the digital system is supplied with power from a variable output voltage power supply apparatus, changes values of the plurality of control

signals held by the plurality of holding circuits in accordance with a probabilistic search technique so that a basic function of the digital system satisfies prescribed specifications.

Claim 7 (Currently Amended): The digital system described in claim 6, wherein, ~~characterized in that~~ in accordance with a genetic algorithm, the setting means sequentially changes values of control signals held in the holding circuits, searching for optimal control signal values that brings the digital system into a state where its basic function satisfies prescribed specifications.

Claim 8 (Currently Amended): The digital system described in claim 6, ~~characterized in that~~ wherein, in accordance with genetic programming, the setting means sequentially changes values of control signals held in the holding circuits, searching for optimal control signal values that brings the digital system into a state where its basic function satisfies prescribed specifications.

Claim 9 (Currently Amended): The digital system ~~described in any~~ of ~~claims~~ claim 6 ~~to 8~~, ~~characterized in that~~ wherein the change to the plurality of control signals by the setting means is performed while changing an output voltage of the power supply apparatus in steps.

Claim 10 (Currently Amended): The digital system ~~described in any~~ of ~~claims~~ claim 6 ~~to 8~~, ~~characterized in that~~ wherein the change to the plurality of control signals by the setting means is performed with an output voltage of the power supply apparatus in a state of being lower than a design supply voltage value of the digital system.

Claim 11 (Currently Amended): The digital system ~~described in any~~ of ~~claims~~ claim 1

~~to 10~~, ~~characterized in having the~~ further including a power supply apparatus.

Claim 12 (Currently Amended): The digital system ~~described in any~~ of ~~claims~~ claim 1 ~~to 10~~, ~~characterized in that~~ wherein the digital system is constituted as an integrated circuit.

Claim 13 (Currently Amended): The digital system ~~described in any~~ of ~~claims~~ claim 1 ~~to 10~~, ~~characterized in that~~ wherein the digital system is constituted as a circuit board.

Claim 14 (Currently Amended): A method of adjusting clock signal timing of a digital system that carries out digital processing in accordance with a single or a plurality of digital clock signals to perform a prescribed basic function, comprising:

inserting each of a plurality of delay elements into each of a plurality of clock circuits that supply the clock signals in the digital system[[,]] ;

constituting each of the plurality of delay elements by a circuit element that changes a delay time according to a value indicated by a control signal[[,]] ~~and~~ ;

holding a plurality of control signals applied to the plurality of delay elements in a plurality of holding circuits provided in the digital system[[,]] ; and

characterized in that in a state in which the digital system is supplied with power from a variable output voltage power supply apparatus, values of the plurality of control signals held by the plurality of holding circuits are changed by an external apparatus in accordance with a probabilistic search technique so that a basic function of the digital system satisfies prescribed specifications.

Claim 15 (Currently Amended): The method of adjusting clock signal timing of a digital system described in claim 14, ~~characterized in that~~ wherein, in accordance with a

genetic algorithm, the external apparatus sequentially changes values of control signals held in the holding circuits, searching for optimal control signal values that brings the digital system into a state where its basic function satisfies prescribed specifications.

Claim 16 (Currently Amended): The method of adjusting clock signal timing of a digital system described in claim 14, wherein, ~~characterized in that~~ in accordance with genetic programming, the external apparatus sequentially changes values of control signals held in the holding circuits, searching for optimal control signal values that brings the digital system into a state where its basic function satisfies prescribed specifications.

Claim 17 (Currently Amended): The method of adjusting clock signal timing of a digital system ~~described in any of claims~~ of claim 14 ~~to 16~~, ~~characterized in that~~ wherein the change to the plurality of control signals by the external apparatus is performed while changing an output voltage of the power supply apparatus in steps.

Claim 18 (Currently Amended): The method of adjusting clock signal timing of a digital system ~~described in any of claims~~ of claim 14 ~~to 16~~, ~~characterized in that~~ wherein the change to the plurality of control signals by the external apparatus is performed with an output voltage of the power supply apparatus in a state of being lower than a design value of the digital system.

Claim 19 (Currently Amended): A method of adjusting clock signal timing of a digital system that carries out digital processing in accordance with a single or a plurality of digital clock signals to perform a prescribed basic function, comprising:

inserting each of a plurality of delay elements into a plurality of clock circuits that

supply the clock signals in the digital system[[,]] ;

constituting each of the plurality of delay elements by a circuit element that changes a delay time according to a value indicated by a control signal[[,]] ~~and~~ ;

holding a plurality of control signals applied to the plurality of delay elements in a plurality of holding circuits provided in the digital system[[,]]; and

characterized in that in a state in which the digital system is supplied with power from a variable output voltage power supply apparatus, values of the plurality of control signals held by the plurality of holding circuits are changed by a setting apparatus provided in the digital system in accordance with a probabilistic search technique so that a basic function of the digital system satisfies prescribed specifications.

Claim 20 (Currently Amended): The method of adjusting clock signal timing of a digital system described in claim 19, wherein ~~characterized in that~~ in accordance with a genetic algorithm, the setting means sequentially changes values of control signals held in the holding circuits, searching for optimal control signal values that brings the digital system into a state where its basic function satisfies prescribed specifications.

Claim 21 (Currently Amended): The method of adjusting clock signal timing of a digital system described in claim 19, wherein, ~~characterized in that~~ in accordance with genetic programming, the setting means sequentially changes values of control signals held in the holding circuits, searching for optimal control signal values that brings the digital system into a state where its basic function satisfies prescribed specifications.

Claim 22 (Currently Amended): The method of adjusting clock signal timing of a digital system ~~described in any~~ of ~~claims~~ claim 19 ~~to 21~~, ~~characterized in that~~ wherein the

change to the plurality of control signals by the setting means is performed while changing an output voltage of the power supply apparatus in steps.

Claim 23 (Currently Amended): The method of adjusting clock signal timing of a digital system ~~described in any~~ of ~~claims~~ claim 19 ~~to 21~~, ~~characterized in that~~ wherein the change to the plurality of control signals by the setting means is performed with an output voltage of the power supply apparatus in a state of being lower than a design supply voltage value of the digital system.

Claim 24 (Currently Amended): The method of adjusting clock signal timing of a digital system ~~described in any~~ of ~~claims~~ claim 14 ~~to 23~~, ~~characterized in that~~ wherein ~~the~~ a power supply apparatus is provided in the digital system.

Claim 25 (Currently Amended): The method of adjusting clock signal timing of a digital system ~~described in any~~ of ~~claims~~ claim 14 ~~to 24~~, ~~characterized in that~~ wherein the digital system is constituted as an integrated circuit.

Claim 26 (Currently Amended): The method of adjusting clock signal timing of a digital system ~~described in any~~ of ~~claims~~ claim 14 ~~to 24~~, ~~characterized in that~~ wherein the digital system is constituted as a circuit board.

Claim 27(Currently Amended): The method of adjusting clock signal timing of a digital system ~~described in any~~ of ~~claims~~ claim 14 ~~to 18~~, ~~characterized in that~~ wherein the external apparatus is equipped with a computer.

Claim 28 (Currently Amended): The method of adjusting clock signal timing of a digital system ~~described in any~~ of ~~claims~~ claim 19 ~~to 23~~, ~~characterized in that~~ wherein the setting means is equipped with a computer.

Claim 29 (Currently Amended): A recording medium recorded with a processing program executed by the computer in the method of adjusting clock signal timing of a digital system according to claim 27 ~~or claim 28~~ for changing the values of the plurality of control signals held by the plurality of holding circuits in accordance with a probabilistic search technique so that the basic function of the digital system satisfies the prescribed specification.

Claim 30 (New): A recording medium recorded with a processing program executed by the computer in the method of adjusting clock signal timing of a digital system according to claim 28 for changing the values of the plurality of control signals held by the plurality of holding circuits in accordance with a probabilistic search technique so that the basic function of the digital system satisfies the prescribed specification.